CLAIMS

What is claimed is:

1. A method of forming a transistor having source and drain regions within a substrate adjacent a gate stack on the substrate, comprising:

forming a layer of poly-SiGe with carbon over a dielectric layer situated on the substrate;

forming a layer of poly-Si over the layer of poly-SiGe; and

patterning the poly-Si, poly-SiGe and dielectric layers to form the gate stack.

2. The method of claim 1, wherein the layer of poly-Si includes carbon.

3. The method of claim 2, further comprising:

forming a polysilicon seed layer over the dielectric layer; and

patterning the polysilicon seed layer in forming the gate stack.

4. The method of claim 3, wherein the seed layer includes carbon.

5. The method of claim 4, wherein the poly-Si, poly-SiGe and seed layers are patterned *via* an etching process.

6. The method of claim 5, wherein the carbon within the layers changes a passivation material formation and etch rate during the etching process.

7. The method of claim 6, wherein the etching is substantially isotropic due to the change in passivation and etch rate.

8. The method of claim 7, wherein the poly-SiGe layer has a greater etch sensitivity to an etchant utilized to etch the layers in forming the gate structure.

9. The method of claim 8, wherein at least one of the seed layer, poly-SiGe layer and poly-Si layer contains a concentration of carbon between about 0.1 to 1.0 atomic percent.

10. The method of claim 3, wherein the seed layer has a thickness of about 100 Angstroms or less.

11. The method of claim 1, wherein the poly-SiGe layer has a thickness of about 400 to 700 Angstroms.

12. The method of claim 1, wherein the poly-Si layer has a thickness of about 350 to 750 Angstroms.

13. The method of claim 1, wherein the dielectric layer has a thickness of about 100 Angstroms.

14. The method of claim 4, wherein at least one of the dielectric layer, seed layer, poly-SiGe layer and poly-Si layer is formed according to at least one of spin-on techniques, sputtering techniques, growth techniques and deposition techniques.

15. A method of forming a transistor, comprising:

forming a layer of dielectric material over a substrate;

forming a layer of poly-SiGe with carbon over a dielectric layer situated on the substrate;

forming a layer of poly-Si over the layer of poly-SiGe;

patterning the poly-Si, poly-SiGe and dielectric layers to form a gate stack; and

doping exposed portions of the substrate adjacent to the gate stack to form source and drain regions.

16. The method of claim 15, further comprising:

doping exposed regions of the substrate adjacent the gate stack to form source and drain extension regions before forming the source and drain regions, wherein the source and drain extension regions are lightly doped relative to the source and drain regions.

17. The method of claim 16, further comprising:

forming sidewall spacers adjacent the gate structure prior to forming the source and drain regions, but after forming the source and drain extension regions.

18. The method of claim 17, wherein forming sidewall spacers comprises:

forming a layer of insulating material over the gate stack and exposed portions of the substrate; and

selectively removing portions of the insulating material.

19. The method of claim 18, wherein the insulating material comprises at least one of silicon nitride and silicon oxide.

20. The method of claim 15, further comprising:

forming a polysilicon seed layer over the layer of dielectric material; and

patterning the polysilicon seed layer in forming the gate stack.

21. The method of claim 15, wherein the layer of poly-Si includes carbon.

22. The method of claim 21, further comprising:

forming a polysilicon seed layer over the dielectric layer; and

patterning the polysilicon seed layer in forming the gate stack.

23. The method of claim 22, wherein the seed layer includes carbon.

24. The method of claim 23, wherein the poly-Si, poly-SiGe and seed layers are patterned *via* an etching process, and wherein the poly-SiGe layer has a greater etch sensitivity to an etchant utilized to etch the layers.

25. The method of claim 23, wherein at least one of the seed layer, poly-SiGe layer and poly-Si layer contains a concentration of carbon between about 0.1 to 1.0 atomic percent.

26. The method of claim 22, wherein the seed layer has a thickness of about 100 Angstroms or less.

27. The method of claim 15, wherein the poly-SiGe layer has a thickness of about 400 to 700 Angstroms.

28. The method of claim 15, wherein the poly-Si layer has a thickness of about 350 to 750 Angstroms.

29. A method of forming a transistor having source and drain regions within a substrate adjacent a gate stack on the substrate, comprising:

forming a layer of poly-Si with carbon over a dielectric layer situated on the substrate; and

patterning the poly-Si and dielectric layers to form the gate stack.

30. The method of claim 29, further comprising:

forming a polysilicon seed layer over the dielectric layer; and

patterning the polysilicon seed layer in forming the gate stack.

31. The method of claim 30, wherein the seed layer includes carbon.

32. The method of claim 31, wherein the poly-Si and seed layers are patterned *via* an etching process.

33. The method of claim 32, wherein the carbon within the layers deters passivation materials from forming during the etching process.

34. The method of claim 33, wherein the etching is substantially isotropic due to the lack of passivation materials.

35. The method of claim 30, wherein at least one of the seed layer and poly-Si layer contains a concentration of carbon between about 0.1 to 1.0 atomic percent.

36. A transistor comprising:

a gate structure formed over a substrate;

dopant implanted into the substrate adjacent the gate structure to form source, drain, source extension and drain extension regions; and

a channel underlying the gate structure, where some of the dopant may drift as a result of a heat treatment,

where the gate structure comprises:

a dielectric layer over the substrate;

a poly-SiGe layer with carbon over the dielectric layer; and

a poly-Si layer over the poly-SiGe layer.

37. The transistor of claim 36, wherein the layer of poly-Si includes carbon.

38. The transistor of claim 37, wherein the gate structure further comprises:

a polysilicon seed layer over the dielectric layer.

39. The transistor of claim 38, wherein the seed layer includes carbon.

40. The transistor of claim 39, wherein the gate structure is formed by an etching process, and wherein the poly-SiGe layer has a greater etch sensitivity to an etchant utilized in the process.

41. The transistor of claim 39, wherein at least one of the seed layer, poly-SiGe layer and poly-Si layer contains a concentration of carbon between about 0.1 to 1.0 percent.

42. The transistor of claim 38, wherein the seed layer has a thickness of about 100 Angstroms or less.

43. The transistor of claim 36, wherein the poly-SiGe layer has a thickness of about 400 to 700 Angstroms.

44. The transistor of claim 36, wherein the poly-Si layer has a thickness of about 350 to 750 Angstroms.